Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **C**
2. **R**
3. **R-C COMMON**
4. **N. ASTABLE**
5. **ASTABLE**
6. **–TRIGGER**
7. **VSS**
8. **+TRIGGER**
9. **EXT. REST**
10. **Q**
11. **N.Q**
12. **RETRIGGTER**
13. **OSC. OUT**
14. **VDD**

**.071”**

**.076”**

**14 1**

**6**

**5**

**4**

**3**

**2**

**10**

**11**

**12**

**13**

**9 8 7**

**MASK**

**REF**

**CD4047B**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .003” X .003”**

**Backside Potential: VDD**

**Mask Ref: CD4047B**

**APPROVED BY: DK DIE SIZE .071” X .076” DATE: 8/25/21**

**MFG: TIH THICKNESS .017” P/N: CD4047BH**

**DG 10.1.2**

#### Rev B, 7/19/02